IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-30 (Canceled).

Claim 31 (Currently Amended): A nonvolatile semiconductor device comprising:

at least one memory cell;

a bit line connected to the memory cell; and

a bit line control circuit including a capacitor, a MOS transistor, a flip-flop circuit, a first transfer gate connected between the capacitor and the bit line, a second transfer gate between the capacitor and the flip-flop circuit, and a third transfer gate connected between the flip-flop circuit and a gate electrode of the MOS transistor, wherein a source electrode of the MOS transistor is coupled to the capacitor, a drain electrode of the MOS transistor is coupled to a voltage source, and the MOS transistor selectively changes ~~an amount of charges~~ a value of a first data stored in the capacitor according to a voltage level of the gate electrode selectively boosted by a change of the voltage source.

Claim 32 (Previously Presented): The device according to claim 31, further comprising:

a fourth transfer gate connected between the source electrode of the MOS transistor and the capacitor, and

the bit line during a program of the memory cell having one of three potential levels controlled by the flip-flop circuit and the voltage level of the gate electrode of the MOS transistor.

Claim 33 (Previously Presented): The device according to claim 31, wherein each of the first, second and third transfer gates and the MOS transistor is an N-type MOS transistor.

Claim 34 (Previously Presented): The device according to claim 32, wherein the fourth transfer gate is an N-type MOS transistor.

Claim 35 (Previously Presented): The device according to claim 31, wherein data stored in the flip-flop circuit is transferred to the gate electrode of the MOS transistor before the flip-flop circuit senses and stores data on the capacitor.

Claim 36 (Previously Presented): The device according to claim 31, wherein the memory cell comprises a charge accumulation layer.

Claim 37 (Previously Presented): The device according to claim 36, wherein the charge accumulation layer is controlled by a control gate of the memory cell.

Claim 38 (Previously Presented): The device according to claim 31, further comprising:

plural memory cells; and

a NAND cell unit connected in series with the plural memory cells.

Claims 39-45 (Canceled).

Claim 46 (New): The device according to claim 31, wherein the flip-flop circuit latches a second data different from the first data during the MOS transistor selectively changes the value of the first data.